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HUBER, ROBERT T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/589,915	CHONG ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *22-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/01/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1 - 21 in the reply filed on April 28, 2008 is acknowledged. Claims 22 – 34 are withdrawn from consideration.

Specification

2. The abstract of the disclosure is objected to because it is presented on a sheet containing other material (such as information pertaining to the International Publication). Correction is required. See MPEP § 608.01(b).

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Electrically Writeable and Erasable Memory Medium with Layers of Phase Changing Material" or something similar.

Claim Objections

4. Claim 8 is objected to because of the following informalities: The claim recites the total thickness of the individual layers, however it is unclear and ambiguous if the intended meaning is for each individual layer thickness, the thickness of the combination of individual layers in the multiple layer structure, or the thickness of the laminated structure. For purposes of examination the "total thickness of the individual

layers" is interpreted to mean "the total thickness of each multiple layer structure".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 – 9, 11, 12, 15 – 17, 20, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kostylev et al. (US 2004/0026730 A1) of record.

a. Regarding claim 1, **Kostylev discloses a data recording element for a memory cell of a writeable and erasable memory medium** (figure 7) **comprising:**

a laminated structure (laminated structure comprising layers 140a - 140d and 150a – 150d) **of at least two multiple-layer structures** (first multiple layer structure 140a and 150a, second multiple layer structure 140b and 150b, and third multiple layer structure 140c and 150c),

each said multiple-layer structure comprising a plurality of individual layers (each multiple layer structure has at least 2 layers, as disclosed above),

at least one of the plurality of individual layers in each multiple layer structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]),

one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]).

b. Regarding claim 2, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein the plurality of sequentially disposed individual layers are disposed in a same sequence in at least two said multiple-layer structures** (paragraph [0041]).

c. Regarding claim 3, **Kostylev discloses the data recording element as recited in claim 1, wherein the plurality of sequentially disposed individual layers are disposed in a different sequence in at least two said multiple-layer structures** (paragraph [0041]).

d. Regarding claim 4, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein each individual layer has a thickness in a range of about 0.1 nm to about 10 nm** (paragraph [0048] discloses the stabilization layers 150a – 150e to be less than 5nm thick, and paragraph [0053] discloses the programmable resistance material layers 140a – 140d to be less than 17.5 nm thick).

e. Regarding claim 5, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein all the individual layers in each said multiple-layer structure have the same thickness** (paragraph [0048] discloses the stabilization layers 150a – 150e to be less than 5nm thick, and paragraph [0053] discloses the programmable resistance material layers 140a – 140d to be less than 17.5 nm thick, and therefore all layers may have the same thickness).

f. Regarding claim 6, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein any two neighboring individual layers have a ratio of thickness in a range of about 0.1 to about 10** (as disclosed in paragraphs [0048] and [0053]).

g. Regarding claim 7, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein the total thickness of the data recording element is in a range of about 5 nm to about 500 nm** (paragraph [0054] discloses the total thickness is less than 80 nm).

h. Regarding claim 8, **Kostylev discloses the data recording element as recited in claim 7, as cited above, wherein the total thickness of the individual layers is in a range of about 5 nm to 100 nm** (paragraphs [0048] and [0053] discloses the individual layer thickness, which yields a total layer thickness of each multiple layer structure of less than 22.5 nm).

i. Regarding claim 9, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein at least one of the plurality of individual layers is formed of a material selected from a group consisting of Ge, Te, Sb, Ag, GeTe, SbTe, AgIn, GcSbTe, AgInSbTe, TeAsGe, TeSeS, TeSeSb, InSbTe, TeGeSn, In, Cr, N, Se, Sn, Si, Bi and Ag** (paragraph [0050] discloses the programmable resistance layers to comprise Te, Ge, Sb, and other materials).

j. Regarding claim 11, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein a resistance of said at least one individual layer is lower in an crystalline state-than that in an amorphous**

state (Kostylev incorporates U.S. Patent 5,166,758 by reference in paragraph [0049]. Patent 5,166,758 discloses the layers of a phase changing material to have a lower resistance in the crystalline state than in the amorphous state in col. 4, lines 35 - 43).

k. Regarding claim 12, **Kostylev discloses the data recording element as recited in claim 1, as cited above, further comprising a final individual layer** (final individual layer 140d), **disposed upon said at least two multiple-layer structures, said final individual layer being formed of the same material of a first individual layer** (first individual layer 140a) **of a first multiple-layer structure of said laminated structure** (layer 140d may be of the same material as layer 140a, as disclosed in paragraph [0041]).

l. Regarding claim 15, **Kostylev discloses the data recording element as recited in claim 12, as cited above, further comprising an electrode formed adjacent to the data recording element** (electrode 110, disclosed in paragraph [0029]), **an edge of the electrode contacting the data recording element for transferring electrical signals between the electrode and the data recording element** (e.g. as seen in figure 7).

m. Regarding claim 16, **Kostylev discloses the data recording element as recited in claim 1, wherein said laminated structure forms a superlattice-**

like structure (e.g. as seen in figure 7, the structure has alternating layers of phase changing material, and thus is a superlattice, as defined on pages 9 and 10 of the current application's specification).

n. Regarding claim 17, **Kostylev discloses a data recording element for a memory cell of a writeable and erasable memory medium** (e.g. figure 7) **comprising:**

a laminated structure (laminated structure comprising layers 140a - 140d and 150a – 150d) **having a first external layer** (layer 140a), **a second external layer** (external layer 140d) **and a plurality of internal layers** (internal layers 140b, 140c, 150b, 150c, and 150d) formed between the first and second external layers (as seen in the figure), **at least one layer of the laminated structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse** (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]).

o. Regarding claim 20, **Kostylev discloses a memory cell for a writeable and erasable memory medium** (figure 7) **comprising:**

a substrate (substrate 100);

first and second contacts formed on said substrate (contacts 110 and 160, disclosed in paragraph [0035]);

a data recording element formed between said first and second contacts (data recording element comprising layers 140a – 140d, and 150a – 150e),

said data recording element comprising a laminated structure of two or more multiple-layer structures (first multiple layer structure 140a and 150a, second multiple layer structure 140b and 150b, and third multiple layer structure 140c and 150c),

each said multiple-layer structure comprising a plurality of sequentially disposed individual layers (each multiple layer structure has at least 2 layers, as seen in figure 7),

at least one of said individual layer in each multiple-layer structure being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]),

one of the plurality of individual layer having at least one atomic element which is absent from other one of the plurality of individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in

paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]);

a high temperature electrode formed adjacent the data recording element (paragraph [0059] discloses the memory cell to have one or more electrodes, and paragraph [0029] discloses the electrodes to be made of tungsten, which is a high temperature material); **and**

an insulating material isolating said memory cell from adjacent memory cells (dielectric material 120).

p. Regarding claim 21, **Kostylev discloses an electrically writeable and erasable memory medium** (figure 2A) **comprising**

a plurality of memory cells (memory cells 20) **and an arrangement of conductors** (conductors 24) **such that each memory cell is electrically addressable** (as disclosed in paragraph [0025]), each said memory cell (figure 7) **comprising:**

a substrate (substrate 100);

first and second contacts formed on said substrate (contacts 110 and 160, disclosed in paragraph [0035]);

a data recording element formed between said first and second contacts (data recording element comprising layers 140a – 140d, and 150a – 150e),

said data recording element comprising a laminated structure of two or more multiple-layer structures (first multiple layer structure 140a and 150a, second multiple layer structure 140b and 150b, and third multiple layer structure 140c and 150c),

each said multiple-layer structure comprising a plurality of sequentially disposed individual layers (each multiple layer structure has at least 2 layers, as seen in figure 7),

at least one of said individual layer in each multiple-layer structure being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]);

one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]),

a high temperature electrode formed adjacent the data recording element (paragraph [0059] discloses the memory cell to have one or more electrodes, and paragraph [0029] discloses the electrodes to be made of tungsten, which is a high temperature material); **and**

an insulating material isolating said memory cell from adjacent memory cells (dielectric material 120).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kostylev in view of Sandhu et al. (US 5,837,564). **Kostylev discloses the data recording element as recited in claim 1, as cited above, but is silent with respect to at least one of the plurality of individual layers is deposited in a crystalline state. Sandhu discloses that layers of memory material comprising chalcogenides** (Kostylev

discloses the memory material of his device to also comprise chalcogenides such as Te in paragraph [0050]) **may be deposited in a crystalline state** (col. 2, lines 18 – 19).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the individual memory layers are deposited in a crystalline state, since it was known that such memory layers can be formed in such manner, as disclosed by Sandhu. One would have been motivated to make the layers in a crystalline state since it would yield a more consistent and predictable device (Sandhu: col. 2, lines 31 - 35)

10. Claims 13, 14, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kostylev in view of Chen (US 2005/0051901 A1).

a. Regarding claims 13 and 14, **Kostylev discloses the data recording element as recited in claim 12, as cited above, but is silent with respect to wherein a crystallization speed of said first individual layer and final individual layer is higher than that of other layers of the multiple-layer structure, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure. Kostylev is also silent regarding the crystallization temperature of said first individual layer and final individual layer is in a range of 90°C to 120°C. Kostylev does disclose materials which may comprise the phase change memory medium** (paragraphs [0050] - [0052] for the phase change material and paragraphs [0042] - [0047] for the stabilizing layers) **and suggests**

that the layers comprising the phase change memory medium can be arranged in any manner (paragraph [0041]).

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first individual layer** (layer 22d) **and final individual layer** (layer 22a) **is higher than that of other layers** (lattice mismatch layers 24) **of the multiple-layer structure** (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota et al. (US 5,063,097) discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142°C (col. 11, lines 66 - 68), and Miyamoto et al. (US 2004/0106065) discloses the crystallization temperature of GeTe to be 200°C (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and final individual layers have a higher crystallization speed and lower crystallization

temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption, while maintaining structural integrity (as disclosed in paragraph [0055] of Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

With respect to the first and final individual layers having a crystallization temperature within a range of 90°C to 120°C, it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05.

b. Regarding claims 18 and 19, **Kostylev discloses the data recording clement as recited in claim 17, as cited above, but is silent with respect to wherein said first and second external layers having a relatively high crystallization speed and low crystallization temperature than the internal layers. Kostylev is also silent regarding the crystallization temperature of said first and second external layers is in a range of about 90°C to 120°C. Kostylev does disclose materials which may comprise the phase change memory medium** (paragraphs [0050] - [0052] for the phase change material and

paragraphs [0042] - [0047] for the stabilizing layers) **and suggests that the layers comprising the phase change memory medium can be arranged in any manner** (paragraph [0041]).

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first external layer** (layer 22d) **and second external layer** (layer 22a) **is higher than that of the internal layers** (lattice mismatch layers 24) (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota et al. (US 5,063,097) discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142°C (col. 11, lines 66 - 68), and Miyamoto et al. (US 2004/0106065) discloses the crystallization temperature of GeTe to be 200°C (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe)**.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and

final individual layers have a higher crystallization speed and lower crystallization temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption, while maintaining structural integrity (as disclosed in paragraph [0055] of Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

With respect to the first and final individual layers having a crystallization temperature within a range of 90°C to 120°C, it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
May 15, 2008

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892